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To:	Examiner Ann McCamey	**From:**	Kacia Lee
Company:	USPTO	**Date:**	2/24/2004
Fax #:	571-273-2010		
Re:	Rule 132 Declaration in 10/090,796		

Total Number of Pages (including cover): 12

Message

Dear Examiner McCamey:

Our attorney Walter Nielsen had indicated that you did not receive the Rule 132 Declaration that we filed on October 14, 2003. Following is a copy of the Rule 132 Declaration as filed, as well as a copy of the postcard date-stamped in the OIPE. Please let me know if you have any questions, if you do not receive all pages, or if there is anything else we can provide for you--particularly if there are additional items listed on the postcard which did not make their way to you.

Best regards,

Kacia Lee
Paralegal Assistant
612-371-2142

EXPEDITED PROCEDURE – EXAMINING GROUP 2833

S/N 10/090,796 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yuan-Liang Li	Examiner:	Ann M. McCamey
Serial No.:	10/090,796	Group Art Unit:	2833
Filed:	March 6, 2002	Docket No.:	884.A87US1
Title:	SHUNTING ARRANGEMENTS TO REDUCE HIGH CURRENTS IN GRID ARRAY CONNECTORS		
Assignee:	Intel Corporation	Customer No.:	21186

DECLARATION UNDER 37 C.F.R. § 1.132

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

This declaration is submitted under 37 C.F.R. §1.132 prior to any final rejection of U. S. Patent Application Serial Number 10/090,796 to establish that the undersigned inventor was a co-inventor of the subject matter disclosed in U.S. Pat. No. 6,388,207.

I, Yuan-Liang Li, do hereby declare:

1. I have been employed by Intel Corporation from prior to December 29, 2000, the filing date of U.S. Pat. No. 6,388,207, until the present. My current job title is Engineering Manager.

2. I am the inventor of the inventive subject matter of the present application as described, illustrated, and claimed therein.

3. I am a co-inventor of the inventive subject matter of U.S. Pat. No. 6,388,207 as described, illustrated, and claimed therein, as evidenced by the following:

a. Having earlier conceived the claimed subject matter of U.S. Pat. No. 6,388,207 in the United States with the co-inventors, my name appears along with theirs on an Invention Disclosure, a copy of which is attached hereto as Exhibit A (8 pages). The

"Invention Date" deleted from page 1 of Exhibit A is prior to December 29, 2000. Other sensitive information has been blocked out from Exhibit A.

b. Figure 2 of Exhibit A illustrates conceptually a multi-layered substrate comprising a plurality of "trenches" or "shunts".

4. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Date: 10-9-03 Yuan-Liang Li

YUAN-LIANG LI
By His Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation

Date 10/9/2003 By Walter W. Nielsen
Walter W. Nielsen
Reg. No. 25,539

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9th day of October, 2003.

Anne M. Richards Anne M Richards
Name Signature

P9999
15437
TMG/TM/TMG/ATD

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TMG INVENTION DISCLOSURE, Rev 1,
Located at: http://legal.intel.com

LEGAL ID# _____(legal dept. use only) DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JFS-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444.**

Fill out the below and follow the instructions:

1. **Field of the Invention:**
   - **Semiconductor Process: device and integration**
   - **Semiconductor Process + Equipment: thin films**
   - **Semiconductor Process + Equipment: etch/litho**
   - **Circuit Design**
   - **Flash**
   - **Test**
   - **OQN (QAR)**
   - x **Packaging**
   - **Boards/Cartridge**
   - **Automation**
   - **Other**
2. **Concise Title of Invention:** Advanced Hybrid Package Design for Improved Power Delivery, Current Carrying Capability, and Signal Integrity

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3. Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):

The Invention is: The invention is a unique hyorid package design, which combines DC shunting and planes through the core for low inductance power/ground planes and high quality references for signals through the core of a package. This design can be applied to microprocessor, memory and microcontroller packaging and other package applications, which require high-speed power delivery, low inductance, high current carrying capability, and signal integrity or any combination of these items.

The key elements are:

1. High Current Carrying Capability.
2. Low inductance through the core for better power delivery.
3. Single and/or dual reference planes through the core of a package for high quality signals.
4. Embedded passive structure package design with high dielectric materials integrated into various levels of the package, which provides large amounts of capacitance at very low inductances.
5. Can be utilized for all package applications including level 1 (direct connection to microprocessor) or level 2 (motherboard) package applications.
6. Can be used for all material type packages including organic, ceramic, flex and tape.
7. Can be used for all applications requiring power delivery and signal integrity.
8. High capacitance/area with ultra low inductance structure.
9. Design using channels/trenches and/or vias for current carrying or signal reference.
10. Increased current carrying capability.
11. Unique design for shielding signals and addressing power delivery issues.

Note: Applications include microprocessor, memory, microcontroller and chip set. In the succeeding text, detail and descriptions will focus on microprocessor applications. Other applications such as memory and microcontroller and chip set will be similar in detail.

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4. Inventor(s):

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Supervisor M/S: CH5-157
BUM Presenter:
Inventor Signature:

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5. ***HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)***

   DATE: _____ **SUPERVISOR NAME:** Joan Yrla

   BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?**
   If yes, explain and give date: No
   (Give expected tape out date if applicable):

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel? No**
   If yes, explain and give date:

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
   If yes, explain and give date: No
9. **Has this *invention* been conceived, or constructed during accomplishment of a *government* or third party contract? If yes, give contract name and number: No**

10. **Explain the problem being addressed by the invention:**

    This invention addresses the problem of:

    1. Meeting *microprocessor, memory,* chip set and microcontroller inductance requirements for power delivery.
    2. Meeting *microprocessor, memory,* chip set and microcontroller signal integrity requirements through the core of the package using single and dual reference planes.
    3. Meeting *microprocessor, memory,* chip set and microcontroller current requirements by providing dc shunts in the package for current to flow.
    4. Providing a cost-effective solution for power delivery, which includes a low inductance path as well as a low resistive path for dc current, and signal integrity requirements.
    5. *Meeting requirements for increasing microprocessor, memory, chip set and microcontroller* performance while reducing the overal package size.

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11. Explain current state of the art (i.e, how the problem is solved today):

Presently the problem described above is solved by:
There are a number of ways power delivery, inductance and signal integrity issues are addressed today. Typically, current is carried to and form microprocessor, memory, chip set and microcontroller by copper planes/strips formed on the surface of a particular layer and by copper metallization deposited on side walls of plated through holes and vias. Microprocessor, memory, chip set and microcontroller power-delivery performance requirements are addressed by the use of discrete capacitors. These discrete capacitors are mounted on the surface of the package using standard surface mount and reflow processing. As the power, performance and signal integrity requirements increase for microprocessor, memory, chip set and microcontroller package assemblies, increasingly higher numbers of discrete capacitors, smaller diameter vias and thinner traces are needed. This higher number of capacitors utilizes package space, which could be used for signal, power and ground routing. In addition, the large numbers of capacitors that are required add significant cost to the package.

A second problem with this approach is inductance targets cannot be met. Discrete capacitor leads and the long current loops drive inductance to levels, which are above requirements for maximum microprocessor performance. Poor signal references, as a result of referencing PTH vias in the core of a package degrade the performance of the I/O.

A third problem with this approach is that performance requirements drive the number of vias to increase and the trace size to decrease. At the same time, current per trace or via is increasing. As the current levels increase, trace and/or via metallization can overheat, crack or delaminate from the underlying materials leading to degraded performance or failure of the microprocessor, memory, chip set and microcontroller.

A fourth problem is the cost and throughput of the processes used to form vias, trenches and traces for transmission of signals and delivery of power. A typical process would use mechanical or laser drill to form the drilled hole. This drilled hole would then be cleaned and plated with a conductive metallization such as copper. Conductive traces can be formed by several methods such as etching of conductive foil and plating of conductive metallization. Both processes required wet chemistry techniques. Trenches can be formed by routing and/or drilling. Routing process cost and procedures would be very similar to drilling.

Drilling and routing are typically a batch processes. For mechanical drilling and routing, panels are stacked and then drilled or routed. Throughput is dependent on drill or rout bit diameter, material hardness, panel thickness, drill or rout machine parameter settings and other conditions. As the via diameter shrinks or trench dimensions increase, throughput goes down. Laser drilling is done in single panels. The laser beam ablates the panel material in the desired location. Again as the via diameter shrinks, throughput goes down.

Wet chemistry processes process single panels on a conveyor line. Throughput is dependent on size and spacing of traces and spaces, chemistry and equipment settings and panel size. Typically throughput goes down as density increases.

Explain technical advantages of the invention over current state of the art:

The technical advantage of this invention is:
1. *Provides an organic package with high capacitance, ultra low inductance performance and integrity of* signals to insure rise time, propagation speed and impedance requirements are met.
2. Integrates high Dk ceramic material into an organic package.
3. Provides EMI benefits.
4. Allows for more routing space on surface layers.
5. Minimizes total package assembly cost.
6. Allows for standard HDI (high density interconnect) processing to be done on the organic package using this material.
7. Provides capacitance with acceptable breakdown voltage, leakage current and loss properties.
8. Utilizes high volume manufacturing processes.
9. Reduces overall package dimensions.
10. Provides excellent shielding of signals.
11. Addresses Imax concerns with traces, vias and PTH's.
12. Allows for parameter shrink with minimal decrease in throughput.
13. Allows cost effective and high throughput manufacturing of the design(s).
14. Allows the use of low Dk core and build up layer materials.

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13. a. Is the invention experimentally verified?
    b. Is the invention verified with simulation?
    c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

Description: There are 3 distinct electrical advantages that this invention provides and 1 distinct manufacturing advantage. First, trenches are created that provide DC shunts through the package. Second, reference planes are created in the package that help signal integrity. Third, the trenches can be alternate power and ground trenches that are closely spaced to provide low inductance through the core of the package. For the manufacturing advantage, the trenches are created using a router before the plating bath that is used to plate the PTH vias. By doing this, the impact to TPT should be minor because the time spent drilling the PTH vias is traded off for routing time.

First, note that all trenches provide a low resistive path through the core for better current carrying capability. One should note the different trenches available with this invention. There are trenches provided on the outer rim of the package, which could be advantageous for socket designs that would take advantage of this by connecting to the sides of the package. There are trenches that are internal to the package. And there are trenches that are created in the outer wall of the cavities, which contain the embedded capacitors.

Notice the signal PTH vias in this invention which are sandwiched between 2 trenches. The signals, which are normally only surrounded by other vias for reference, can now be surrounded by 2 planes power/ground, power/power, or ground/ground. This provides a strip-line configuration. In addition, a microstrip can also be achieved by placing the vias close to just a single trench/plane.

Notice the closely spaced planes on the right side of "Figure 2. Invention". These closely spaced trenches/planes provide a low inductance path through the core.

A number of techniques can be used to form vias, traces and trenches and apply conductive metallization. Traditional methods such as mechanical or laser drilling can be used. Newer techniques such as imprinting and microperforation can be used. A secondary benefit to imprinting and microperforation is that low Dk liquid crystal polymer (LCP) material can be used for core and build up layers for organic substrates. Low Dk LCP materials provide benefits to signal transmission speed. Plus coefficient of therm expansion (CTE) can be tailored to more closely match the CTE of the die. Thus reducing the emechanical stress on the die and substrate structure.

A typical process to manufacture the designs shown above would be:

1. Form required via holes, trenches, spaces and traces in the core layer(s) using imprinting and microperforation.
2. Clean residue from vias and trenches using plasma or other cleaning techniques.
3. Fill trenches and vias with conductive filler.
4. Plate conductive metallization to complete trace build up as necessary.
5. Apply build up layer material to core.
6. Repeat process for forming, cleaning and metalizing vias, trenches, traces and spaces until all build up layers have be formed..
7. Note, lamination or curing of the build up layers will need to be done. This can be done sequentially or all at once.

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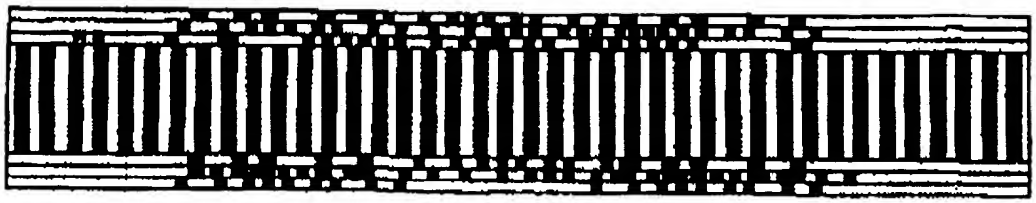
15.

Cross section view



TOP VIEW

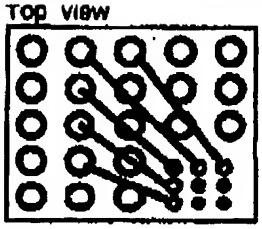


Figure 1. Prior Art

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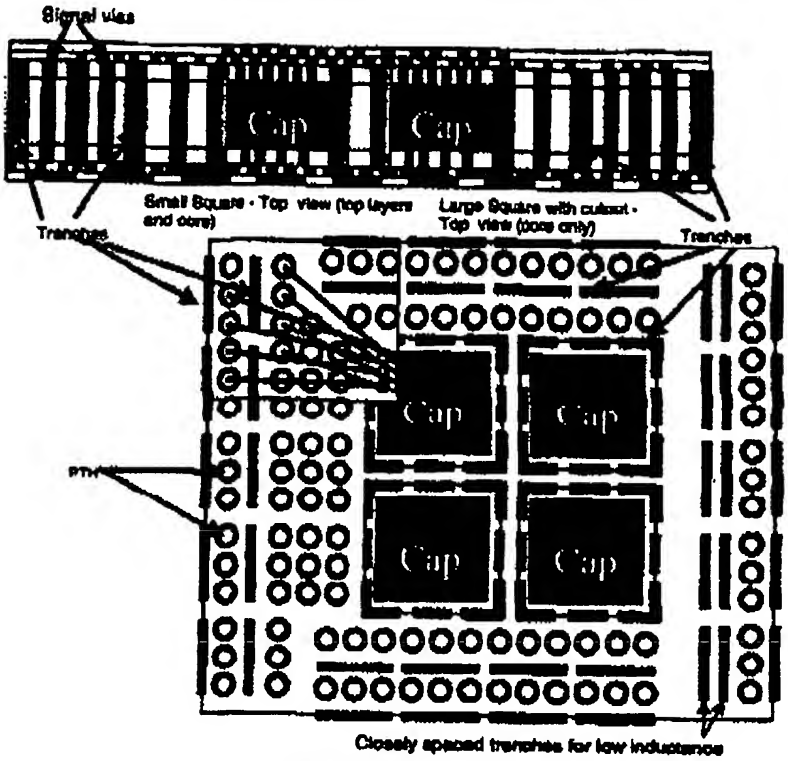

Figure 2. Invention

16. **Key Supporting Data (1 page limit on separate page):**

17. **What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):** Next generation microprocessor, memory, chip set and microcontroller packages.

18. **Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name:** _____

19. **Any other information IP committee should consider?**